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The plasmonic memristor: a latching optical switch

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Plasmonic memristors are electrically activated optical switches with a memory effect. This effect is important for a new generation of latching optical switches that maintain their state without power consumption. It is also of interest for new optical memories that can be activated by a single electrical write/erase impulse. The operation principle is based on the reversible formation of a conductive path in the dielectric layer of a plasmonic metal–insulator–metal waveguide. Extinction ratios of 12 dB (6 dB) are demonstrated in 10 μm (5 μm) long devices for operating voltages of ±2 V. With this, the devices feature the characteristics of electronic resistive random access memory, but for the field of plasmonics. Such plasmonic memristors are interesting in view of new applications in information storage and for low power circuit switching. © 2014 Optical Society of America

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Integrated optically readable memories are key elements in the toolbox of next-generation information storage, as they permit one to replace electrical data buffers in optical communication systems [1]. Moreover, latching optical switches are needed for low power circuit switching [2].

Memory switching effects have been studied in electronics for many years [3–5]. One important example is the so-called resistive random access memory (RRAM or ReRAM) or memristor (memory resistor). RRAMs have attracted attention as possible candidates for future nonvolatile memories as an alternative for today's flash memories. Typical devices consist of a capacitor-like metal–insulator–metal (MIM) structure. The two states of RRAMs are accessed by applying a voltage between the two metals. Depending on the voltage, either a high-resistance or low-resistance nanometer-scale conductive path is formed in the insulator between the two metals.

In plasmonics, the signal is encoded as a surface plasmon polariton (SPP) that propagates along a metal–dielectric interface. The confinement of such SPP modes may be below the diffraction limit, which is why the field of plasmonics has triggered a number of suggestions for small-scale switch implementations [6–12]. Most interestingly, the typical structure of a RRAM device with its MIM layers also could serve as a plasmonic MIM waveguide and, thus, might pave the way for a new resistive switch in the field of plasmonics. Combining RRAMs with plasmonics allows one to relate the electrical and the optical world with new applications in circuit switching and memory concepts and ultimately could lead to the realization of a compact latching switch with electrical write/erase and optical readout functionality. Recently, optical switching with a 0.09 dB extinction for the first time indicated the feasibility of a plasmonic RRAM device [13]. The device consisted of a silver/amorphous silicon/p-silicon layer structure with the resistive switching being caused by the formation and annihilation of a metallic filament in the amorphous silicon layer. In another demonstration, a thermally induced insulator–metal phase transition based on vanadium dioxide was used to demonstrate plasmonic switching with a memory effect [14]. With this scheme, the authors showed a rather high extinction ratio of 10.3 dB with a device of 5 μm length. The device, however, requires relatively high electrical powers of about 28 mW for the thermally induced phase change.

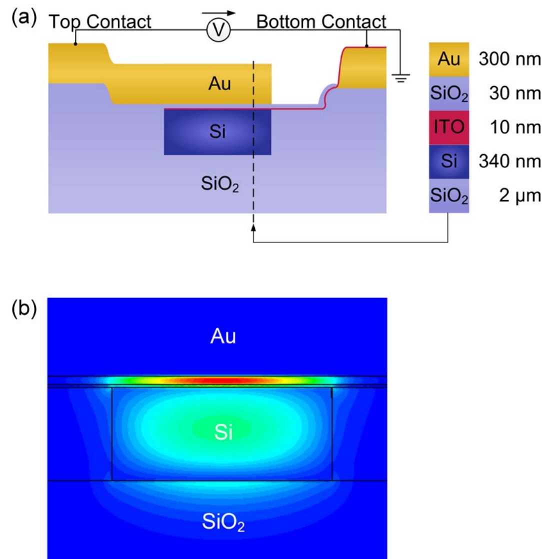

Fig. 1. (a) Cross-sectional view of the plasmonic memristor. The device comprises the typical memristor MIM layers that further serve as a plasmonic waveguide (gold/silicon dioxide/ITO) on top of a silicon photonic waveguide. (b) Electric field distribution of the quasi-TM fundamental mode in the hybrid plasmonic and SOI waveguide. The mode is highly confined in the 30 nm thin SiO_2 layer. When applying a voltage, a conductive path is formed in the insulating layer that strongly perturbs the plasmonic mode.

In this work, we present a plasmonic memristor with a high extinction ratio. More precisely, we demonstrate a latching optical switch based on the electrically induced creation and elimination of a conductive path in a gold/silicon dioxide/indium-tin oxide layer structure. The device is integrated with a silicon photonic waveguide and performs switching with an extinction ratio of 12 dB (6 dB) for a 10 µm (5 µm) long device. The operation power is consumed only when the state of the switch is changed and is below 200 nW.

The resistive switch consists of a hybrid waveguide with a plasmonic section on top of a silicon photonic strip waveguide (800 nm × 340 nm), as suggested in [9,11]. This hybrid approach allows for a simple fabrication process and can be easily integrated with a silicon photonic platform designed for TM polarization. Figure 1(a) shows the cross section of the device. The plasmonic waveguide itself is formed by a 30 nm thick silicon dioxide (SiO_2) layer sandwiched between a 10 nm thick indium-tin oxide (ITO) layer and a 300 nm thick gold (Au) layer. The ITO layer has a nominal carrier concentration of 10^{19} cm^{-3}. It is thin to enable coupling between the photonic and plasmonic sections. Figure 1(b) shows the corresponding electric field distribution of the quasi-TM fundamental mode at 1550 nm wavelength obtained with numerical simulations using the commercial software CST Microwave Studio. In this structure, a significant part of the electrical field is confined to the thin SiO_2 layer (39%). This is crucial for memristor performance, since the optical field has to interact with tiny nanofilaments in the insulator. Simulated propagation losses and coupling losses between the silicon photonic and the hybrid waveguide section are 0.2 dB/µm and 1.2 dB per interface, respectively. The ITO layer and the top metal further serve as bottom and top electrodes, respectively. They are connected to metal pads for contact with electrical probes. The ITO bottom electrode is contacted via a 300 nm thick Au layer at the side of the photonic waveguide; see Fig. 1(a). Light is coupled to the memristor by means of silicon strip waveguides with TM grating couplers at both ends.

The silicon photonic structures are fabricated on a silicon-on-insulator (SOI) substrate with a 340 nm thick silicon layer and 2 µm thick buried oxide layer using a single step e-beam lithography and an inductively couple plasma reactive-ion etching (ICP-RIE) process. The chip is then covered by a plasma-enhanced chemical vapor deposition (PECVD)-grown 500 nm thick SiO_2 layer acting as cladding for the photonic waveguide. Local openings in the SiO_2 on top of the photonic waveguides (1.6 µm wide) define the plasmonic sections of the devices. They are fabricated via photolithography and an RIE process. The 300 nm Au bottom contact is produced using photolithography, e-beam evaporation and a lift-off process. This contact is laterally offset with respect to the photonic waveguide. Next, the 10 nm ITO layer is RF-sputtered and structured using photolithography and lift-off. A 30 nm SiO_2 layer is RF-sputtered on top. A second 300 nm Au contact is deposited and structured similarly to the bottom one. Finally, the 30 nm oxide is opened locally using an RIE process to access the bottom contact pad. Figure 2 shows an optical microscope image of a fabricated device.

The device was characterized in two steps. First, we studied the quasi-static behavior. We measured the hysteresis of the current and the optical transmission while slowly sweeping the applied voltage. In a second step, we investigated the time-resolved switching process.

We measured the current and the optical transmission as a function of the applied voltage. As indicated in Fig. 1, the voltage was applied between the top and bottom electrodes. A compliance current of 100 nA was set to protect the device from permanent breakdown. Continuous-wave laser light at a wavelength of 1550 nm was coupled to the chip through grating couplers. The transmitted optical signal was measured with a powermeter.

The electrical behavior of a 5 µm long device with the laser being turned off is displayed in Fig. 3. The applied voltage was swept from −3 to 3 V and back in steps of 60 mV with

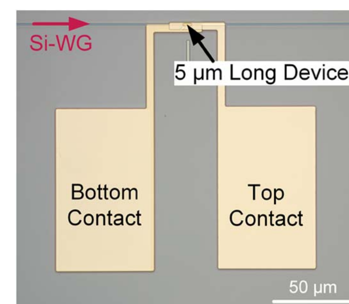

Fig. 2. Optical microscope image of the 5 µm long plasmonic switch. Light is coupled by means of a silicon waveguide (Si-WG) to the plasmonic memristor. The golden squares are the electrical contact pads.

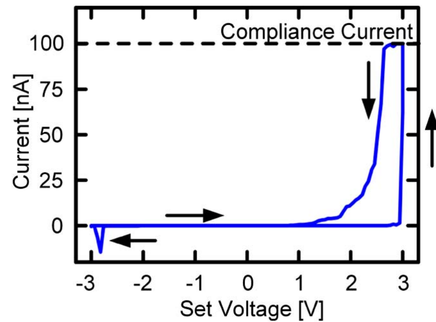

Fig. 3. Electrical current–voltage characteristic of the plasmonic memristor. The response indicates a hysteresis as it is typical for resistive switching memory cells. An abrupt increase of the current is found with a threshold around 2.9 V. Note that the set voltage differs from the actual (measured) voltage in the compliance limit.

a duration of 2 s per step. We observed a sudden increase of the current at a threshold of ~2.9 V. Here, the current reached its compliance limit. When scanning back, the current decreased while showing a hysteresis. This hysteresis is typical for RRAM devices [5].

Figure 4(a) shows the normalized optical transmission for 50 consecutive measurement cycles below threshold (±2 V, 20 mV per step, 2 s per step, total duration of 13.3 min per cycle). We started at −2 V in the ON state. While gradually increasing the voltage, the optical signal decreased. When decreasing the voltage, the optical transmission increased again, while being lower than for the forward sweep direction. This hysteresis indicates the memory effect of the switch. The device returned to its initial state after completion of each measurement cycle. This shows excellent repeatability of the switching effect. The difference between the ON and OFF states (extinction ratio) was 6 dB. The latching extinction ratio between the latched states was 3.5 dB. Since the device was operated below threshold, no significant current was measured and no hysteresis was observed in the I–V curve. Therefore, peak operating power during switching is below 200 nW.

The dependence of the extinction ratio on the device length was investigated, as well. From Fig. 4(b) one can see that increasing the length from 5 to 10 μm increases the extinction ratio from 6 to 12 dB. Thus, the extinction ratio increases with increasing device length. While two devices with different lengths do not yet provide sufficient statistics, the result at least indicates a trend.

Propagation losses in the hybrid waveguide section of 1 dB/μm and coupling losses between the silicon photonic and the hybrid waveguide of 6.5 dB per interface were determined through cut-back measurements. The experimentally determined losses are higher than the simulated ones due to fabrication imperfections. When opening the silicon dioxide cladding to define the plasmonic section, the structure was overetched. This resulted in a step between the silicon photonic and the hybrid waveguide sections, explaining the high coupling losses. The same process step led to surface roughness at the top of the silicon waveguide that contributed to the propagation losses. Furthermore, layer imperfection, in particular in the sputter-deposited silicon dioxide layer,

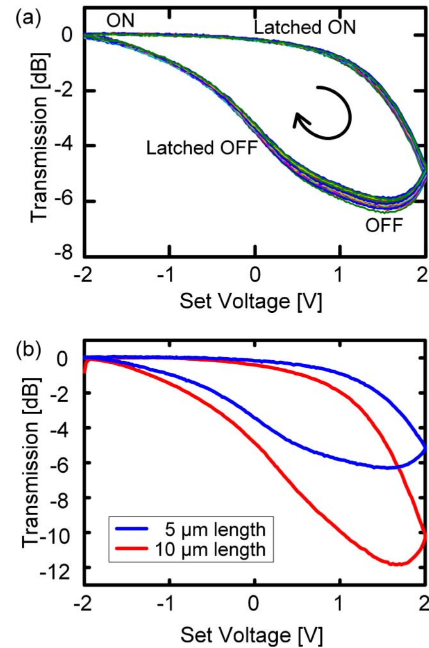

Fig. 4. Quasi-static performance of the plasmonic memristor. (a) Latching optical switch behavior for a 5 μm long device: 50 measurement cycles of the normalized optical transmission as a function of the set voltage showing hysteresis and an extinction ratio of 6 dB. (b) Latching optical switch behavior of a 10 μm long device showing an extinction ratio of 12 dB. During these measurements below threshold, no hysteresis was observed in the I–V curve.

influenced the propagation losses. Better control of the fabrication process will avoid this problem for future devices.

The results of Figs. 3 and 4 can be explained as follows. When a positive voltage is applied, a conductive path is formed in the oxide layer. As this conductive path is bridging the two electrodes, the current increases. For the reverse scanning direction, the conductive path is eliminated, so that the current decreases. Since the plasmonic signal is highly confined in the insulating layer, it is quite sensitive to the alteration of the insulating layer. This is why the switch may be operated below threshold. Even before electrical switching, the plasmonic mode is strongly perturbed by the conductive path, thus reducing the optical transmission.

A change of the ITO refractive index due to carrier accumulation/depletion was also said to influence the optical transmission [9,11]. However, theoretical calculations predict low extinction ratios (~1 dB) [9], so this effect is considered to be small compared to the resistive switching.

The physical nature of the resistive switching mechanism was reviewed in literature and is still not fully understood [3,5]. Yet, it is known that defects in insulating layers, such as metals and oxygen vacancies, play an important role in resistive switching devices, as they enable the formation and elimination of the conductive path. In the present device, the sputter-deposited SiO_2 that is used as an insulating layer is expected to contain a large number of defects [15]. For comparison, a sample with PEVCD SiO_2 was fabricated showing much lower extinction ratios and no hysteresis in the voltage-transmission curve. The switching mechanism

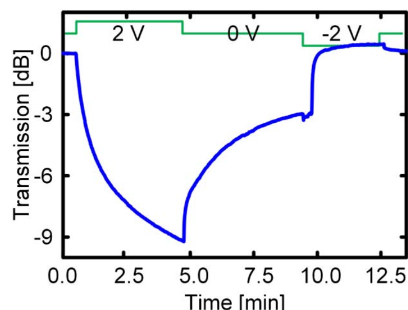

Fig. 5. Dynamic behavior for a 5 min switching process. A voltage of 2 V was applied for 5 min, before switching the voltage off again (green). A latching extinction ratio of 3 dB was observed. By applying a voltage of −2 V. The device was reset to its initial state.

might be explained by positively charged ions being injected from the top electrode. The ions thereby form narrow conductive filaments. This metal filament type of resistive switching was even observed with *in situ* transmission electron microscopy studies [15]. The layer thicknesses of the present plasmonic memristor are too small to resolve nanofilaments in a scanning electron microscopy study. However, needle-like gold filaments were reported in a very similar structure with a 100 nm thin sputter-deposited silicon dioxide layer in the supplement file of reference [16]. Another switching mechanism suggested in the literature is based on a conductive path of oxygen vacancies that is formed in the oxide layer. In that sense, silicon dioxide might be utilized by locally enriching silicon inside the silicon oxide matrix [15,17–20].

To further assess the device, we studied the dynamic behavior of the switch. Here, we determined the step response of the device at both minute and millisecond time scales. Moreover, a megahertz modulation was applied to the device.

The slow switching process is depicted in Fig. 5. A voltage of 2 V was applied to a 5 μm long device for 5 min, before switching the voltage off again. The optical signal measured with a power meter showed a latching extinction ratio of 3 dB. After that, the device was reset to its initial state by a negative voltage of −2 V.

Furthermore, a 5 ms long electrical impulse of 2 V was applied to the optical memristor (see Fig. 6). Here, the optical response of a 20 μm long device was measured with a photodiode and a real-time oscilloscope. Despite the short duration, a latching switching behavior was found as well. The latching extinction ratio was ~0.6 dB, however. Thus, the extinction ratio increases with the duration of the pulse that is applied. The energy required for a transition is as little as 60 μJ or 1 nJ, depending on the switching duration.

To further investigate the switching speed, a sinusoidal modulation in the megahertz regime was applied to the device and detected with a photodiode and a lock-in amplifier. This revealed a relatively flat frequency response between 40 kHz and 10 MHz. The 3 dB bandwidth at an operation with ±2 V with respect the amplitude at 40 kHz is 30 MHz (see Fig. 7, blue triangles). However, subnanosecond switching times have been reported for electronic memristors [21].

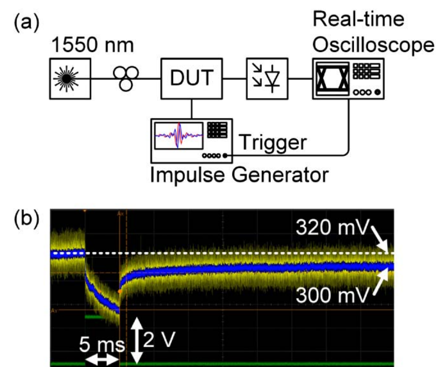

Fig. 6. Dynamic behavior for a 5 ms switching process. (a) Measurement setup: an electrical impulse was sent to the device under test (DUT) while measuring the optical response with a photodiode on a real-time oscilloscope. (b) Screenshot of the real-time oscilloscope showing the switching process (yellow) for a 5 ms long electrical impulse of 2 V (green). The blue line is the measured signal after a low-pass filter. A latching extinction ratio of ~0.6 dB was observed.

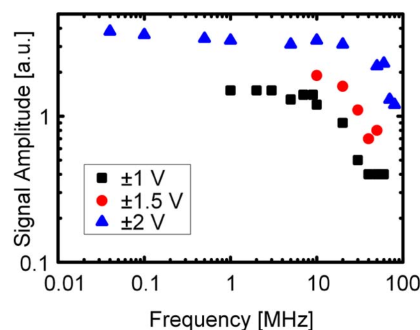

Fig. 7. Megahertz frequency response of the plasmonic memristor. A sinusoidal signal was applied to a 5 μm long device using an arbitrary waveform generator. The optical signal was detected with a photodiode and a lock-in amplifier.

Higher speeds thus should be doable for plasmonic memristors with optimized dimensions and material compositions.

In conclusion, we demonstrated a latching optical switch that combines the memristor concept with plasmonics. The switch exploits the formation and elimination of a conductive path in the insulating layer of a metal–insulator–metal layer stack. The conductive path leads to an attenuation of the optical mode in the OFF state and is ruptured when switching to the ON state. The plasmonic switch is integrated with a silicon photonic waveguide. Optical extinction ratios of 12 dB at 1550 nm wavelength are shown for 10 μm long devices. The operation power is consumed only when the state of the switch is changed and is below 200 nW with operating voltages in the range of ±2 V and currents below 100 nA. Tests with 50 write cycles and sinusoidal modulation in the megahertz regime demonstrate excellent repeatability of the switching mechanism.

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